High Voltage Cascaded Step-Up DC-DC Marx Converter for Offshore Wind Energy Systems

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Keywords

«Emerging technology», «Wind Energy», «Converter circuit», «HVDC», « Multilevel converters », «Soft switching».

Abstract

This paper presents an improved cascaded DC-DC resonant converter for offshore windfarms. The improvements are reduced losses and the number of components. The topology is based on the Marx principle where charged capacitors are charged in parallel and discharged in series to achieve the voltage transformation. The four inductors of the converter are designed to resonate with the capacitors to create resonance forcing current zeros to enable zero current switching thereby reducing switching losses. The operating principles and design considerations of the proposed converter are discussed and the design equations are presented. In order to evaluate the operation of 50 MW converter aimed at connecting a 30 kV DC Busbar in a wind power collection system to a 360 kV high voltage DC bus for transmission to the onshore grid was simulated and the results are presented.

Introduction

Due to the increased distances to off shore windfarms from the shore, it is expected that the use of High Voltage Direct Current (HVDC) transmission and Medium Voltage Direct Current (MVDC) distribution systems for the grid integration of windfarms will grow worldwide. One of the key components in such systems is the DC-DC converter, required to act as the interface between the generation, transmission and distribution voltage levels [1]. Well-established DC-to-DC converters based on pulse width modulated (PWM) converters, which require high frequency switching, are not suitable. Application to high voltage, high power systems mean series connection of devices and high power losses [2]. Hence, such converters are not technically and economically feasible.

Some converter topologies, which are suitable for high-voltage operation, have been proposed in the literature. Laird [3] and Alagab [1] have proposed suitable step-up converters. The drawback of these converters is the limited voltage gain. The coupled inductor boost converter and cascaded boost converter presented by Hu [4] and Noui [5] has the advantage of low input current ripple, but its efficiency decreases with increasing power and its switching frequency is high.

Siwakoti, [6], has presented a high step-up DC–DC converter based on a switched coupled inductor arrangement. The converter draws a continuous current from the source, and its voltage gain is controlled by the duty-cycle. A step up resonant converter was introduced by Parastar [7]; the drawback of this converter is the high voltage across the passive components and large power device conduction losses. Modular multilevel converters (MMC) [8]-[9] are proposed for HVDC connected offshore wind

farms. However, the number of IGBT switches is high. The MMC requires a complex capacitor voltage balancing control scheme.

Recently, the common types of Switched Capacitor Converters (SCC) based on the Marx principle have been considered as an alternative topology. The Marx principle allows the realization of a high voltage gain by connecting the capacitors that are charged in parallel and reconnected in series to discharge. Maneiro [10] presented a shunt HVDC tap using a step down DC to DC converter. This arrangement rquires a large number of IGBT switches.

Veilleux [11,12] DC-DC resonant converter topologies based on the Marx principle, although performs well, the conduction losses are relatively high due to the large number of IGBTs. Improvements were made to reduce the number of IGBTS through a multistage arrangement

Etienne Veilleux Cascaded topology

As depicted in Fig. 1, there are multi stages of the Marx modules connected in cascade comprising three main sections of input, middle and output section. The middle section consists of three stages, stage 1, stage 2, and stage 3. Stage 1 and stage 3 are identical but the size of the components are different and every stage consists of two capacitors, three switches, two diodes and an inductor. Stage 2 has three capacitors, four switches and three diodes. The overall DC voltage gain is 2x3x2= 12, (1:12). In addition, there is an output capacitor at the output stage to smoot the load voltage. The operation can be divided into two sub-commutations.

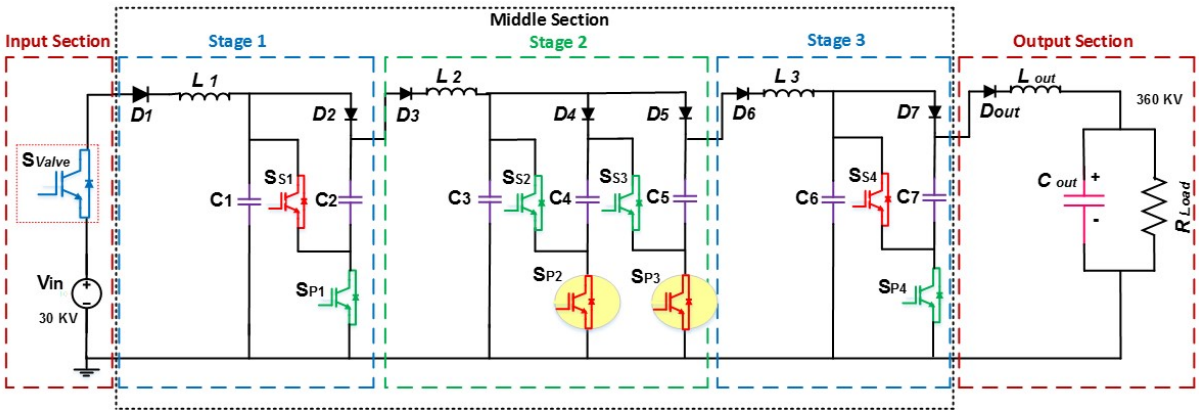

Fig. 1: Veilleux Cascaded Marx DC-DC converter

The charging currents flow through L_1 and L_3. There are no currents in L_2 and L_{out}. In the second sub-commutation, capacitors in stages 1 and 3 are connected in series and discharge to stage 2 and the output section respectively. Stage 2 capacitors are connected in parallel during this period. The charging currents flow through L_2 and L_{out}. There is no current flow in L_1 and L_3.

The process is repeated periodically transferring the electric charges from the input voltage V_{in} to the load R_{load} via stages 1, 2, and 3. A disadvantage of this topology is the high number of IGBT switches in stage 2, and the increasing voltage stress in the IGBTs in successive stages.

Proposed topology

Structure of Cascaded Converter

The structure of the proposed Cascaded DC-DC converter as depicted in Fig. 2 is derived from the Etienne Veilleux converter by modifying the middle section. The advantage is that the number of components are reduced as shown later in the document and the flexibility for increasing the number of stages in the middle section for increasing the gain. The ratings and the component values used for this study are determined for application to the HV converter in a typical wind energy system [Fig. 6]. Fig. 2 shows the equivalent circuit. The input section consists of an input DC voltage source of magnitude V_{in} = 30 kV and HV valve (S_{valve}) comprising series connected IGBTs. The middle section is composed of three stages; stage 1, stage 2 and stage 3. The number of capacitors in stages 1, 2 and 3 are set to 2,

3, and 2 respectively to create a voltage amplification of 2x3x2= 12. However, in general, the number of capacitors can be J, K and L respectively and hence; C_J, C_K and C_L indicate the capacitances in the stages 1, 2, and 3 respectively.

The switching components in the middle section denoted by Ssi (i=1-4) are used to connect the capacitors in series. The IGBT switches denoted by S_{Pi} (i=1-3) are used to connect the capacitors in parallel. The diodes are used to trap the charges in the capacitors and to ensure that they discharge in the correct direction. The output section consists of an output diode D_{out} connected in series with the output inductor L_{out}, and one output capacitor C_{out}. The load is modeled by a pure resistor R_{load}.

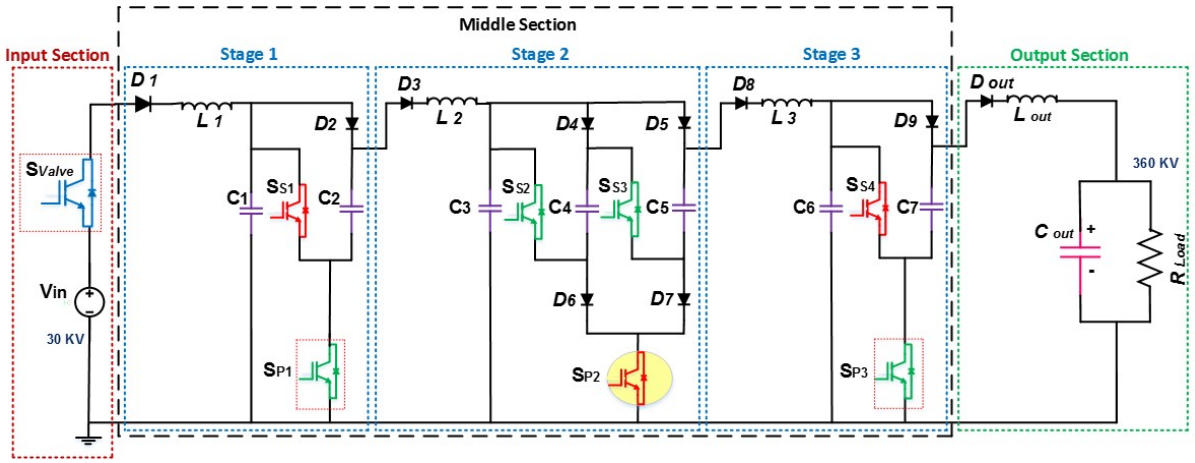

Fig. 2: Improved Cascaded Marx DC-DC Converter

Steady State Operation

The steady state operation can be explained in terms of two sub-commutations. In simple terms, the IGBTs are switched so that the charges in capacitors are pumped from left to right sequentially resulting in a high voltage at the converter output. The switching of the devices are summarised in Table I. The corresponding sub-circuits are shown in Fig 3 and Fig 4, respectively where the ON and OFF devices are shown in green and light grey, respectively. During the first sub-commutation, capacitors in stages 1 and 3 are connected in parallel and are being charged through the inductors L_1 and L_3. The capacitors in Stage 2, which have been charged in the previous cycle are in series and discharges into stage 3 capacitors. Diodes D_1, D_2, D_8 and D_9 conduct.

Table I: IGBT switching logic for the improved converter

Switches	S_{Vlave}	S_{P1}	S_{P2}	S_{P3}	S_{S1}	S_{S2}	S_{S3}	S_{S4}	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{out}
First sub commutation	1	1	0	1	0	1	1	0	1	1	0	0	0	0	0	1	1	0
Second sub commutation	0	0	1	0	1	0	0	1	0	0	1	1	1	1	1	0	0	1

In the second sub commutation the devices are switched so that capacitors in stage 1and 3 and stage 2 are in parallel and series respectively. Hence, capacitors in stages 1 and 3 and 2 are charged and discharged respectively. Repeated switching results in continuous transfer of charge from input side to the output side resulting in a voltage gain of 12, which is equal to the product of number of capacitors (2x3x2) in each stage. The corresponding voltage and current waveforms are given in Fig. 5

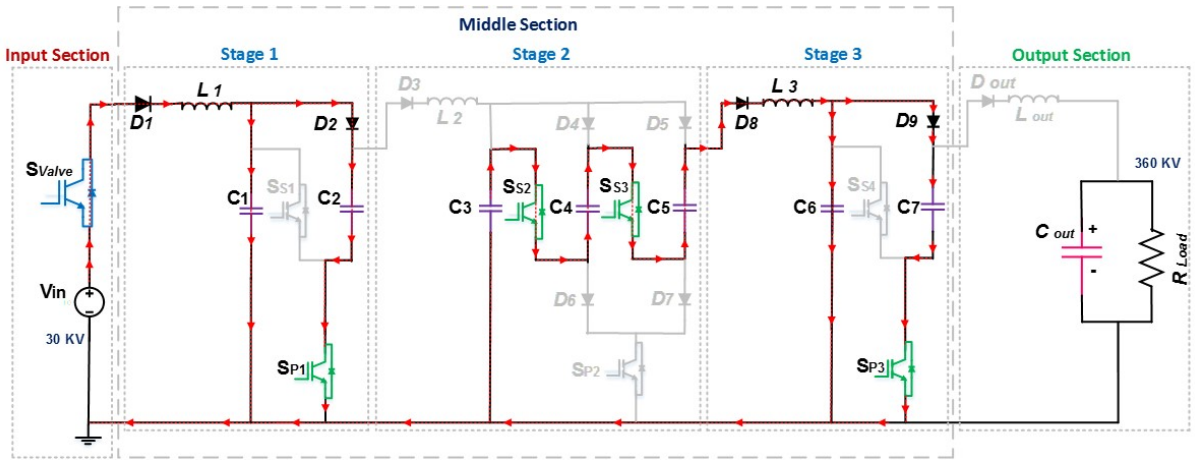

Fig. 3: First sub-commutation configuration

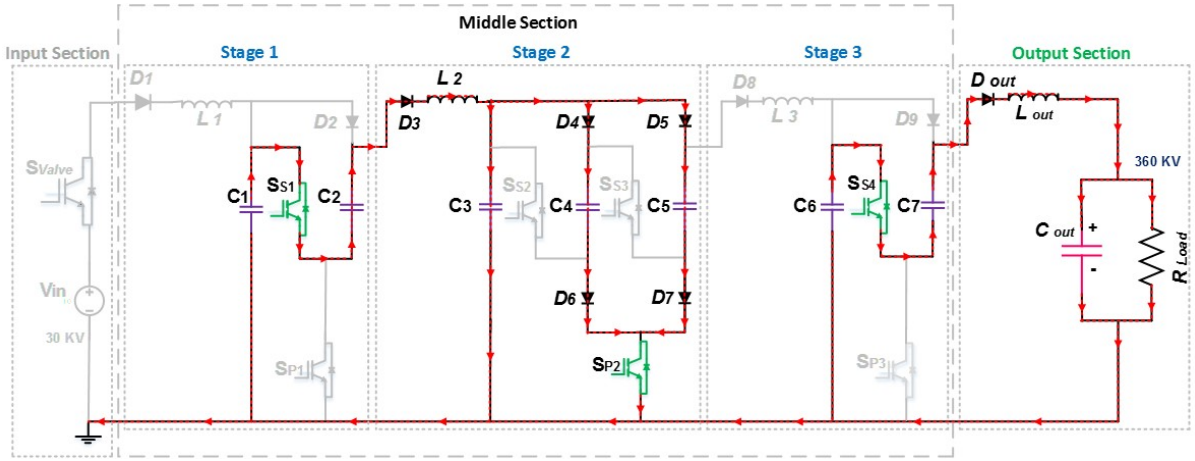

Fig. 4: Second sub-commutation configuration

Generalised analysis of the steady state operation

It is assumed that the cascaded DC-DC converter has already reached steady state. The gain of the converter is depended on the number of capacitance cells in stage 1 (J), stage 2 (K), stage 3 (L). The voltage transformation ratio N is given as;

$$N = \frac{V_{out}}{V_{in}} = J\,K\,L \tag{1}$$

where V_{out} and V_{in} are the output and input voltages, respectively. The equivalent capacitance in stage 1 is

$$C_{eq(J)} = \sum_{J=1}^{J} C_j \tag{2}$$

where C_J is the capacitance, and $C_{eq(J)}$ is the equivalent capacitance of parallel connected capacitors in stage 1. During the first-commutation, the inductor L_1 and the equivalent capacitance $C_{eq\,(J)}$ forms an oscillatory L-C circuit and hence the current in the stage 1 is given by,

$$i_{L1} = i_{Ceq\,(J)} = \frac{V_{in}}{\omega L_1} \sin(\omega t) \tag{3}$$

and

$$\omega = \frac{1}{\sqrt{L_1 C_{eq(J)}}} \tag{4}$$

where $i_{Ceq\,(J)}$ is the current in $C_{eq\,(J)}$. As shown in Fig. 5(a), the peak current in the inductor I_{L1}^{P} can be deduced form the equation (3);

$$I_{L1}^{P} = V_{in}\sqrt{\frac{Ceq\,(J)}{L_1}} \tag{5}$$

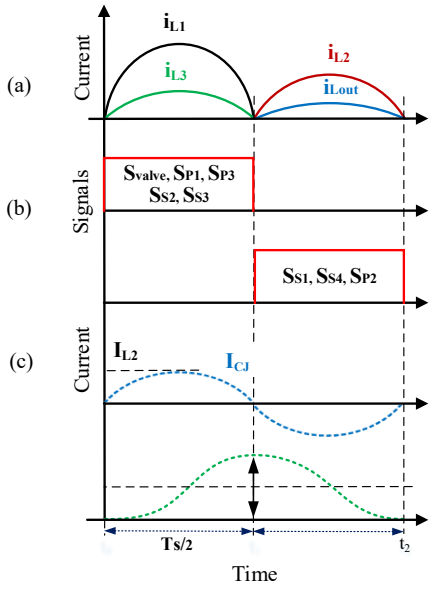

Fig. 5: Ideal steady state waveforms

In order to achieve soft switching, the IGBTs must be switched at the resonant frequency of the inductor current waveform. Therefore, the switching frequency can be written as;

$$F_S = \frac{1}{2\pi\sqrt{L_1 C_{eq\,(J)}}} \tag{6}$$

Determination of stage 1 parameters

The charge transferred to the capacitors in stage 1 can be expressed as;

$$Q = I_{AV}\, T_S \tag{7}$$

where I_{AV} is the average of current in inductor L_1 and T_S is the switching period. Assuming no losses within the converters, it can be shown that

$$Q = \frac{P_{rated}}{NV_{in}}\, T_S \tag{8}$$

where P_{rated} is the rated power, Q is the amount of charge in the switching period and $T_S = (1/F_S)$. Hence,

$$Q = \frac{P_{rated}}{NV_{in}\, F_S} \tag{9}$$

From Fig. 5(d), the charge transferred to stage 1capacitors results in a voltage change of ΔV_{CJ}, which is given by;

$$\Delta V_{C(J)} = \frac{Q}{C_{eq\,(J)}} \tag{10}$$

Substituting for Q from equation (9) to equation (10) and rearranging;

$$C_{eq\,(J)} = \left(\frac{P_{rated}}{NV_{in}\ \Delta V_{C(J)}\ F_S}\right) \tag{11}$$

Hence,

$$C_J|_{j=1,\,J} = \left(\frac{P_{rated}}{NV_{in}\ \Delta V_{C(J)}\ F_S}\right)\ \frac{1}{J} \tag{12}$$

Substituting for F_S from equation (6) into equation (9) and rearranging L_1 can be expressed as;

$$L_1 = \frac{1}{C_{eq\,(J)}}\ \left[\ \frac{Q\,NV_{in}}{2\pi\,P_{rated}}\ \right]^2 \tag{13}$$

Determination of stage 2 parameters

Capacitance values in stage 1, 2 and 3 are chosen so that percent ripple on all the capacitors are the same. This means:

$$C_K\ = \frac{C_J}{J+K+L} \tag{14}$$

In order to ensure soft switching the resonant frequency in the second sub-commutation must be made equal to ω. Hence,

$$\omega = \frac{1}{\sqrt{L_2\left[C_{eq\,(J)} + C_{eq\,(K)}\right]}} \tag{15}$$

where ω is the resonant Frequency of the converter and $C_{eq\,(K)}$ is the equivalent capacitance of both stages C_J in series and C_K in parallel. As shown in Fig.4, the number of capacitors in stage 2, (K) are connected and charged by the number of series capacitors in stage 1 (J). Therefore, the equivalent capacitance of this state is given as;

$$C_{eq}\ = \frac{(C_J/2)(3C_K)}{(C_J/2)+(3C_K)} \tag{16}$$

By combining Equation (15) and (16), equation (17) can be written as:

$$L_2 = \left(\frac{2K^n}{C_{eq(K)}}\right)\left(\frac{C_J}{J^n}\right)^2 \tag{17}$$

Determination of stage 3 parameters

The capacitors in stage 3 is given by equation (19), and in the same way of inductor L_2 was derived, Inductor L_3 can be obtained as;

$$L_3 = \left(\frac{2L^n}{C_{eq(L)}}\right)\left(\frac{C_K}{K^n}\right)^2 \tag{18}$$

and

$$C_L\ = \frac{C_K}{J+K+L} \tag{19}$$

Although, two capacitors are shown in Fig. 2. In general, there can be J capacitors. Therefore, capacitance in the stage 1 is denoted by C_J. Similarly, number of capacitor in the stage 2 and stage 3 are denoted by C_K and C_L, respectively.

The relationship between ripple voltage and capacitor voltage in the first stage is the same in stages 2 and 3, and can be shown as:

$$\frac{\Delta VC_J}{VC_J} = \frac{\Delta VC_K}{VC_K} = \frac{\Delta VC_L}{VC_L} \tag{20}$$

Determination of output section parameters

As illustrated in Fig. 4, the output stage is charged from (t_0-t_1), and the electric charge in stage 3 is transferred in series to the output capacitor C_{out} through an output inductor L_{out} and an output diode D_{out}. The size of the output inductor depends on the output voltage and the amount of charges that needs to be transferred. The value of output inductor depends on the peak-to-peak of output current ΔI_{Lout} can therefore be expressed as;

$$L_{out} = \left(\frac{NV_{in}\, T_s}{\Delta I_{Lout}}\right) \tag{21}$$

The output voltage waveform is not similar to the other voltage capacitor waveforms in the middle stage. Nevertheless, the value of the output capacitor depends on the relation between the amount of charge to the load at half period of time $T_S/2$ and the voltage ripple on the output capacitor. Furthermore, the output capacitor works as charge storage for continuous delivery to the load. The equation can be written as:

$$C_{out} = \frac{\left(P_{rated}/V_{out}\right)\left(T_S/2\right)}{2\pi\, \Delta VC_{out}} \tag{22}$$

Simulation studies

The arrangement and location of the proposed converter is shown in Fig. 6, which forms the basis for the simulation study. In this topology, the cluster is formed by two parallel lines of wind turbines, each containing 5 wind turbines in series. Hence, there is a total of 10 wind turbines; each rated at 5 MW, 1.2 kV [13],[14]. Therefore, the cluster bus voltage is 6 kV and the rated power is 50 MW. The medium voltage (MV) DC-DC converter boosts the voltage from 6 kV to 30 kV. A submarine cable is used to connect the MV converter platform to the main bus of the HV converter.

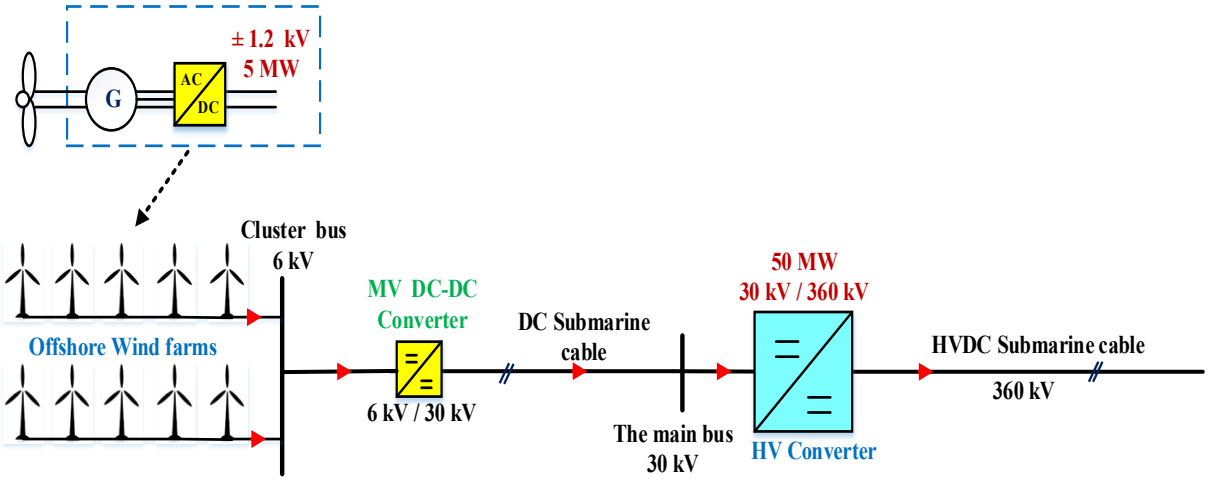

Fig. 6: Electrical system for the Grid Connection of a Windfarm

The HV converter, whose equivalent circuit is shown in Fig. 2, was simulated by Matlab/Simulink software package. The converter parameters (Table II) were calculated using the design equations derived in the previous section.

Table II: Parameters used for cascaded DC-DC converter simulation

Parameter			Value/ model
Number of stages	n		3
Number of capacitors in each stage	J K L		2, 3, 2
Input Voltage	V_{in}		30 kV
Output Voltage	V_{out}		360 kV
Load Current	L_{out}		138.89 A
Rated power	P_{rated}		50 MW
Switching Frequency	F_S		2 kHz
Output Load Resistance	R_{Load}		2592 Ω
IGBT			5SNA 1200G450300
Fast recovery diode			5SDF13H4501
Capacitors		Inductors	
C_J	694.5 µF	L_1	5.3 µH
C_K	99.21 µF	L_2	40 µH
C_L	14.17 µF	L_3	400 µH
C_{out}	300 µF	L_{out}	2.2 mH

Current waveforms in Fig. 7(a) shows the resonant nature of the currents through inductors and IGBTs allowing soft switching at current zeros leading to a reduction in switching losses. Figure 7(b) shows the switching signals clearly indicating soft switching at a frequency of 2 kHz.

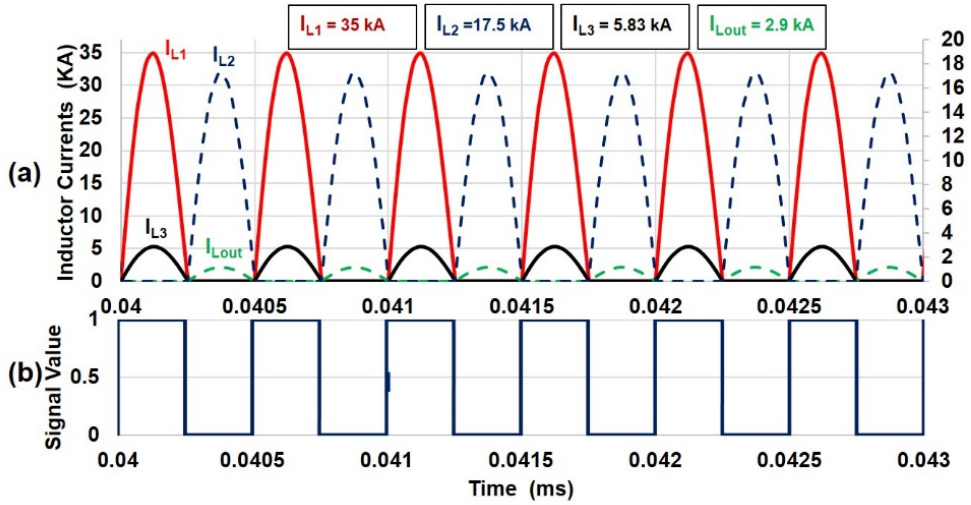

Fig. 7: Matlab / Simulink Simulation results. a) Inductor current waveforms (ZCS), b) switching pattern

Fig. 8 shows the load voltage and current waveforms confirming that the design specifications are met. The DC amplification gain of the simulation is 11.96, which is very close to the design value of 12. The resonating inductor current, which flows through the IGBT increases to a peak I_{L1}= 35 KA in 250 µs, which is within the capability of modern IGBTs [15]. As seen from Fig. 7, the respective peak inductor currents in consequent stages decrease according to the number of capacitors in the previous stage. The effect can be generalised as shown in Table III. The proposed cascaded configuration is evaluated and compared with Veilleux converter in terms of the power device count to highlight its advantages in high-voltage applications. The high voltage with a maximum blocking voltage rated up the ratings of the IGBT considered for this study are 4.5 kV and 1200 A. The total number of IGBTs

can be reduced from 52 to 38 by combining the function of 2 IGBT switches (S_{P2}-S_{P3}) to be performed by 2 diodes and 1 IGBT (Svalve) as illustrated in the yellow circle in Fig.2.

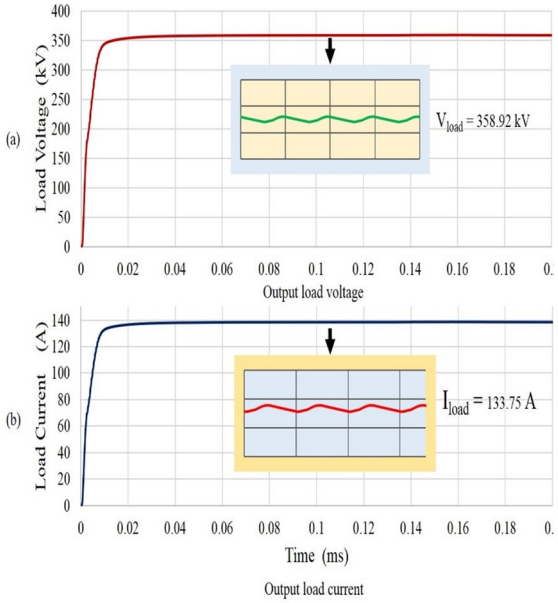

Fig. 8: Simulation waveforms of the improved topology

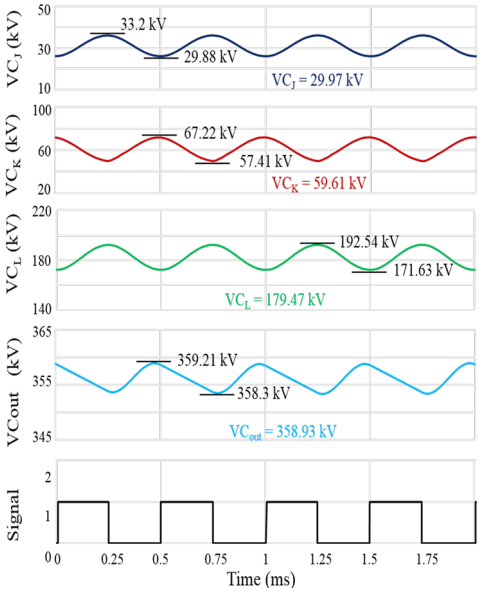

Fig. 9: Simulation results Capacitor voltage waveforms

Table III: shows the peak inductor currents and voltage across capacitors

Parameters	Stage 1	Stage 2	Stage 3	Output section
Number of capacitors	*2*	*3*	*2*	*1*
Peak inductor currents relation	I_{L1}	$I_{L2} = I_{L1}/2$	$I_{L3} = I_{L2}/3$	$I_{Lout} = I_{L3}/2$
Number of stages	*J*	*K*	*L*	L_{out}
Peak inductor currents	I_{L1}^{P}	$I_{L2}^{P} = I_{L1}^{P}/J$	$I_{L3}^{P} = I_{L2}^{P}/K$	$I_{out}^{P} = I_{L3}^{P}/L$
Voltage cross capacitors	$V_{C1}=V_{C2}=V_{in}$	$V_{C3}=V_{C4}=V_{C5}=JV_{in}$	$V_{C6}=V_{C7}=JKV_{in}$	$V_{out}= JKLV_{in}$

As shown in Fig. 9, the average DC voltages a cross capacitors increase and their values depend of the number of capacitors in each stage as depicted in the Table III. Capacitor voltage in stage 1, stage 2, and stage 3 is charging by 29.97 kV, 59.69 kV and 179.47 kV, respectively. The discrepancy between design charging voltage and simulation results is mainly due to small resistance of the IGBT switches and diodes, which have been omitted in the mathematical analysis equations but it is included in the simulation.

Fig. 10 shows that the output voltage in the improved converter is higher than that of Veilleux converter, but both topologies perform equally well. Several HV DC-DC topologies that have a high gain ration, but not always with reduced number of semiconductor component as one of the major goals. Therefore, the improved topology concentrated on reducing the number of devices.

The total number of devices for varying voltage gains are shown in Fig. 11 that shows the device count comparison with different gains between the Veilleux Cascaded converter and the improved cascaded converter. For both configuration, IGBT switches are comprised of several series connected power devices to withstand the rated voltage.

Fig. 11 shows the comparison of designs to give voltage gains of 1:12, 1:27, and 1:36. The number of reduces by 27%, 30% and 37% as the gain increases by 12, 27, and 36, respectively. However, the diode count increases by a small margin. However, diodes are cheaper and easy to connect in series.

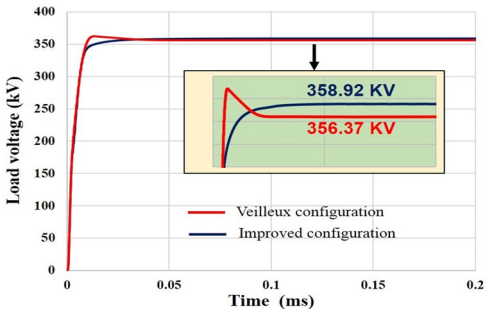

Fig. 10: Load voltage comparisons between Veilleux converter and improved converter

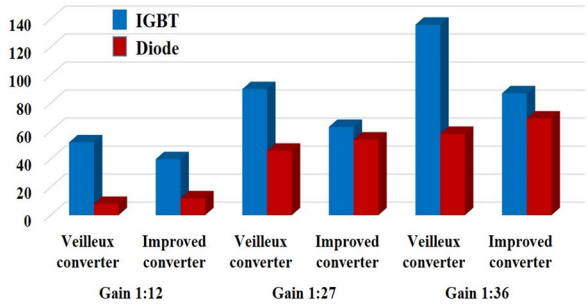

Fig. 11: Components count for DC-DC converter topologies comparisons between Veilleux converter and improved converter

Conclusions

In this paper, the analysis, design and simulation of a high voltage cascaded DC-DC converter using a multi-stage topology suitable for HVDC offshore wind farm applications is presented. This converter can achieves gain with reduced components. The reduction increases with the increase in voltage gain. Soft switching can be implemented and a method for calculating the resonant component values and the switching frequency is given. A design methodology and equations for the determination of the circuit components and solid-state devices is presented. The theoretical predictions have been confirmed by the simulations.

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